



1/6

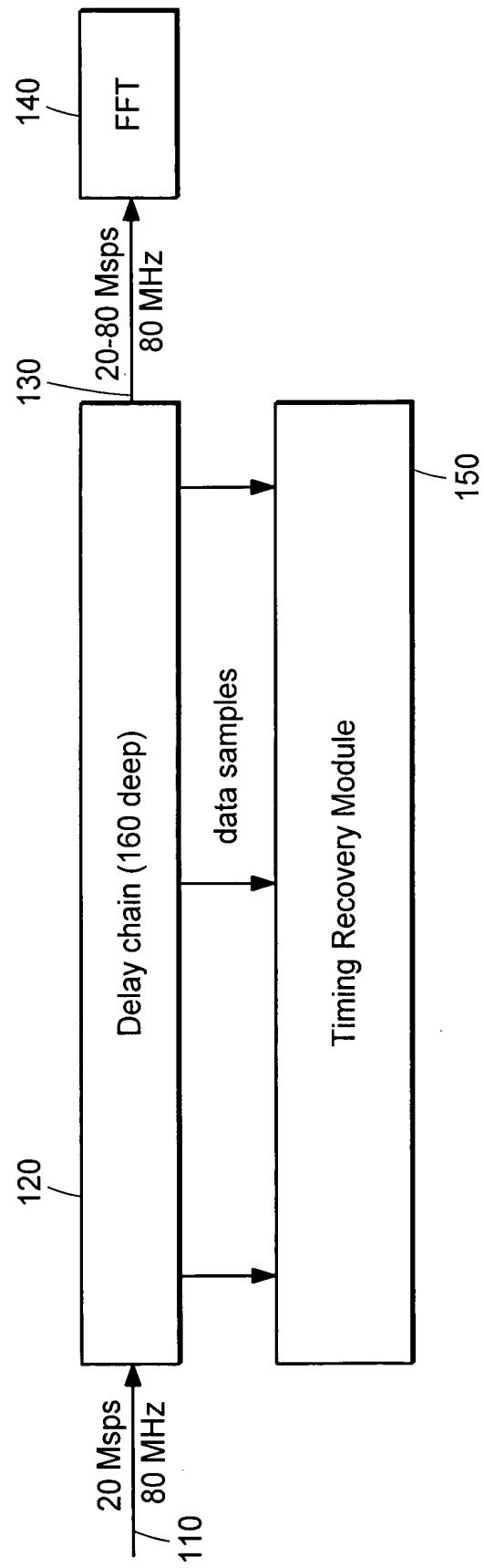


FIG. 1

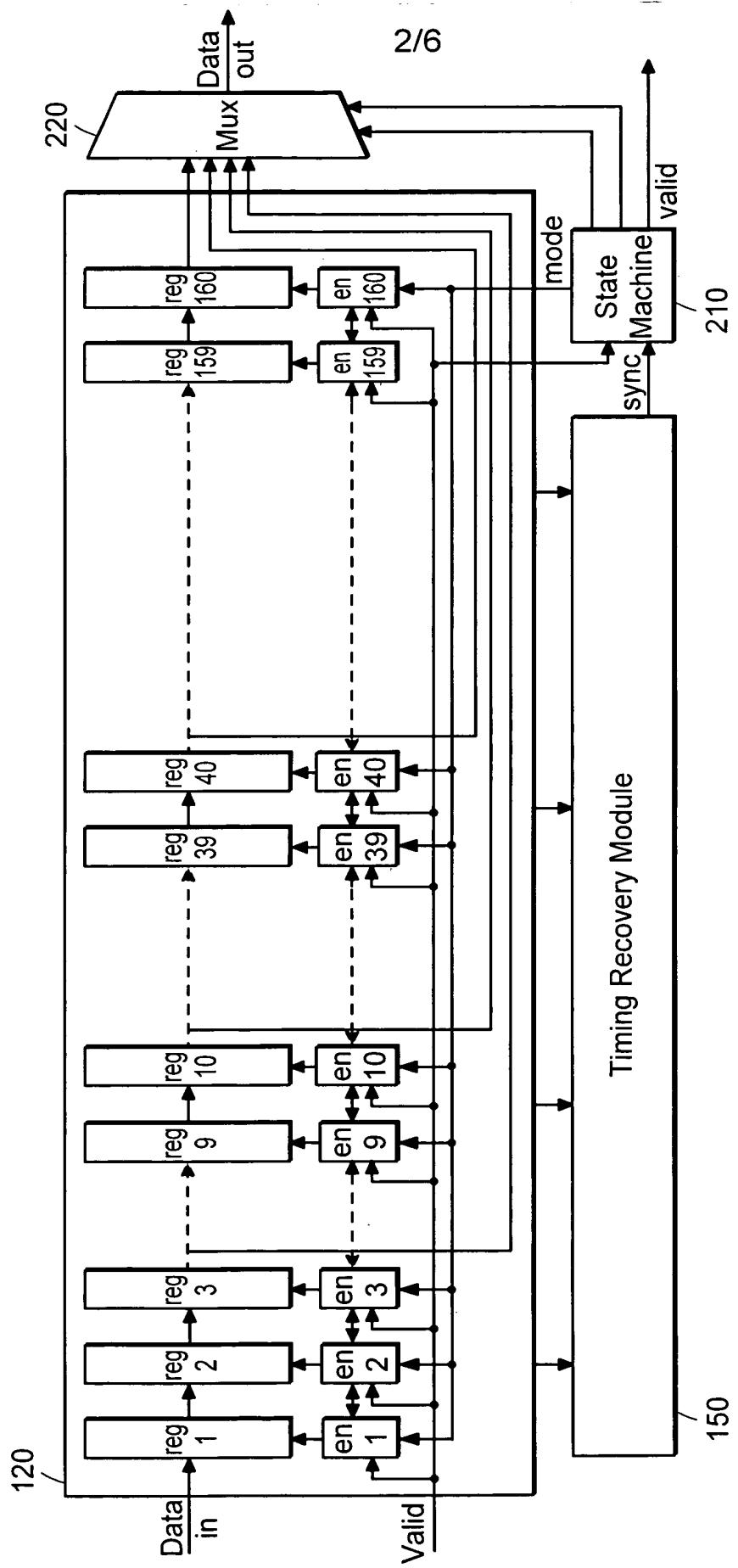


FIG. 2

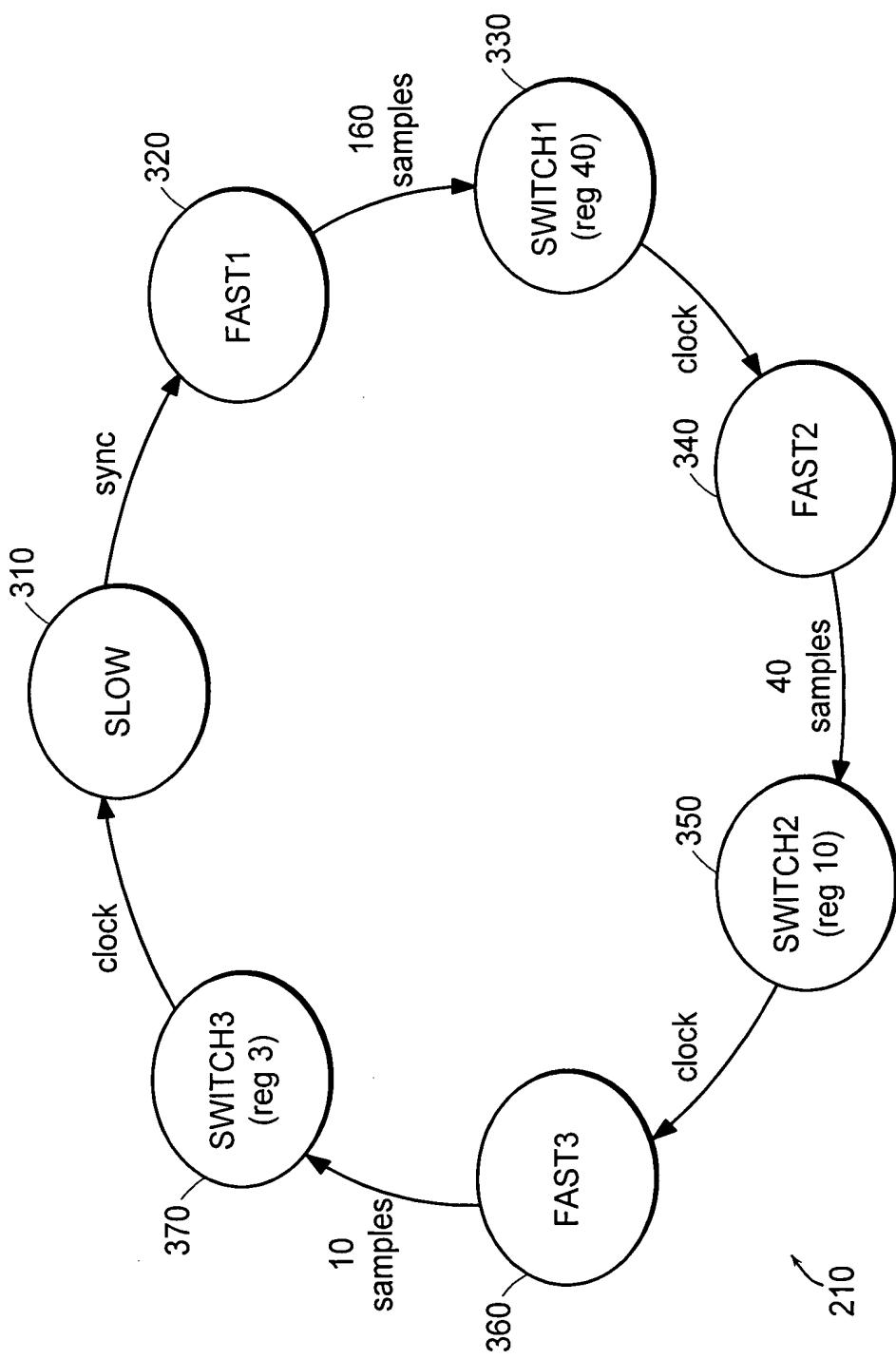


FIG. 3

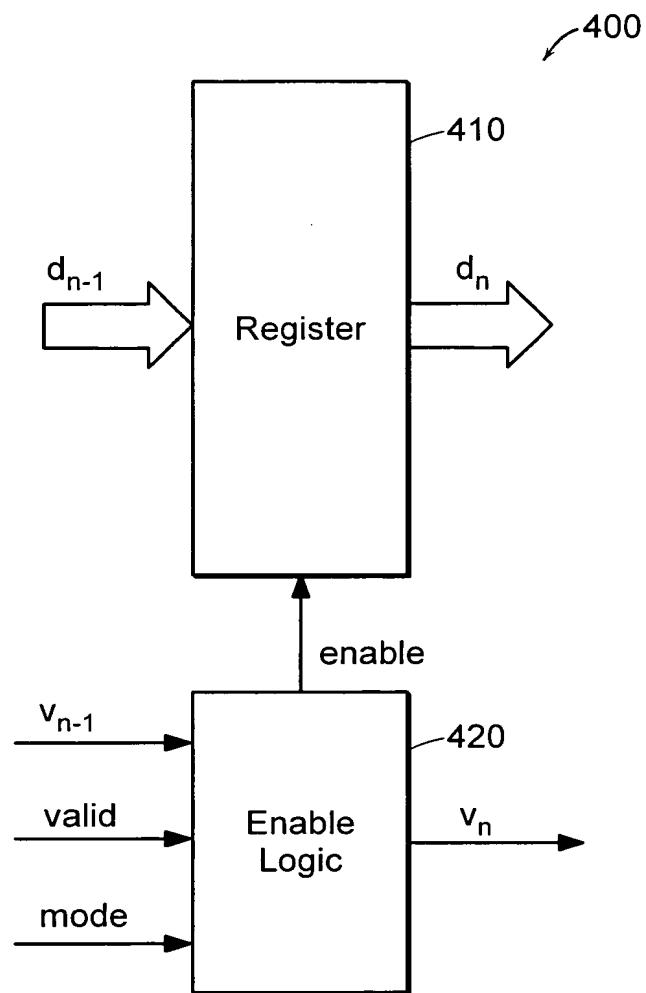


FIG. 4

Clock Cycle	Valid Signal (Incoming Sample at Delay Chain Input)	REGISTERS																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SLOW mode	1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	2	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	3	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	4	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	5	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	6	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	7	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	8	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	9	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	10	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
FAST mode	11	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	12	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	13	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	14	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	15	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	16	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	17	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	18	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	19	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	20	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

FIG. 5

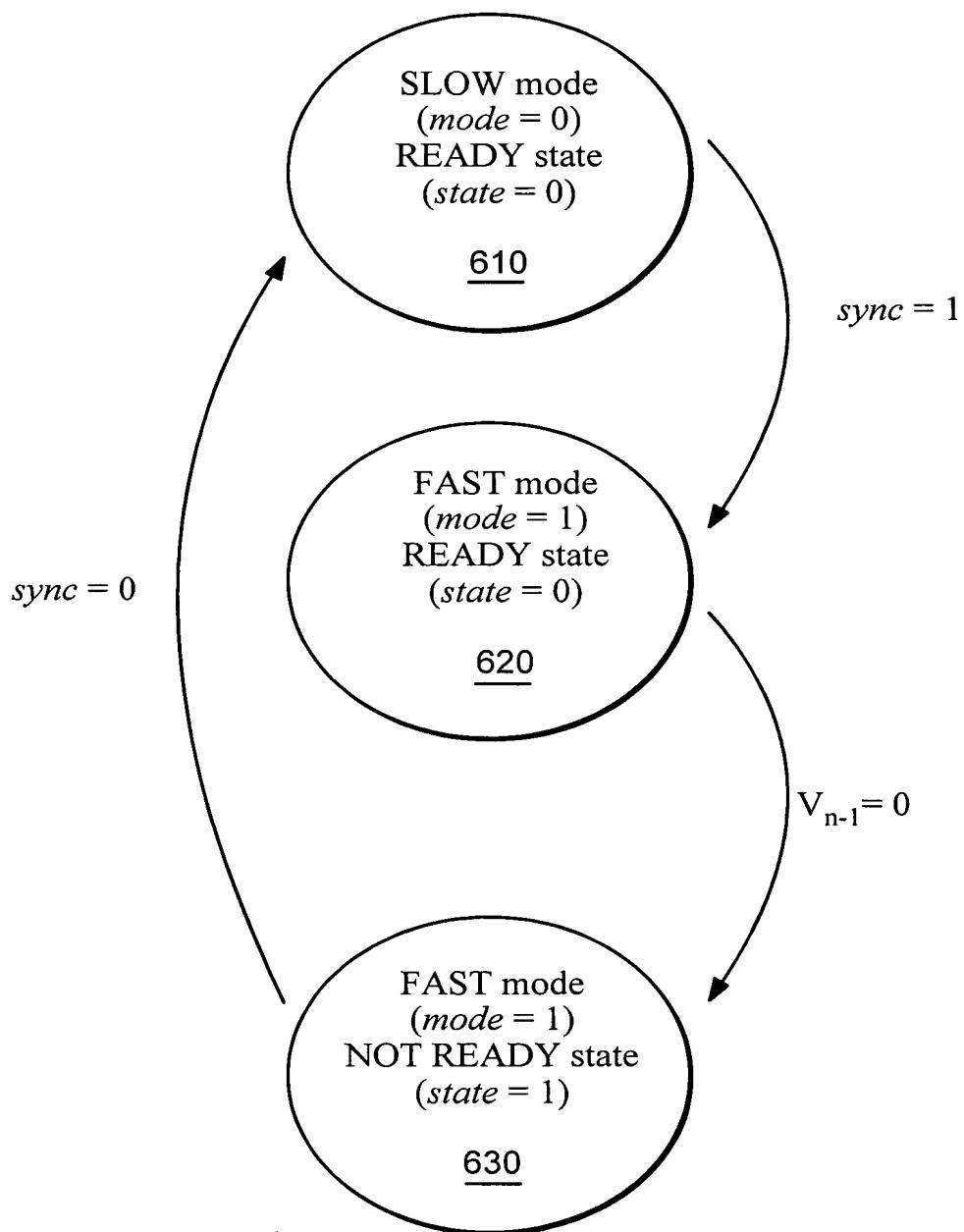


FIG. 6